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Datasheet: SSD PCIe Gen3 x4 Controller AS2263

Version 01.04

Document Controller Center

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Contents

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1. Foreword

This document has been produced by ASolid Technology Co., Ltd., should the company modifies the contents of this specification, it will be re-released with an identifying change of release date and an increase in revision number as follows:

Revision mn.xy, where:

- mn   the first two digit are incremented for major changes of substance, e.g., functional changes.
- xy   the second two digits are incremented when minor changes have been incorporated into the specification, i.e., enhancements, corrections, updates, etc.

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2. Statement of Scope

  This Data Book describes the main features and the applications of SSD PCIe Gen3 x4 Controller For more details, please contact service.asolid@asolid-tek.com directly.

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3. General Description

AS2263 SSD PCIe Gen3 x4 Controller is produced to build Solid-State Drive (SSD) related NAND flash storage devices. All ASolid's flash modules – for both commercial and industrial use, designed with the AS2263, are vibration-free and consume as little power as possible due to its lack of mechanical moving parts. Integrating SMART into the AS2263 completely minimizes the effort to migrate from R&D to mass production, resulting in reduced design-to-market cycles and greater business profits.

The embedded 32-bit microcontroller can provide a high performance of wear-levering and buffer management, and also act as a search engine for its neighboring flash unit. More importantly, ASolid optimal algorithm for wear-leveling can effectively increase the lifespan of a flash chip, especially for MLC, TLC and QLC flash. Moreover, the AS2263 contains Low Density Parity Check (LDPC) of Error Correction Code (ECC) circuitry, which is for increasing data reliability while reading raw data inside a flash chip.

The AS2263 has 16 hardware pins for general input/output control. These 16 pins can be programmed individually for input or output application. Furthermore, the default level of these pins is used for default function settings of the controller, the type of flash, and the PICe speed setting. The AS2263 also supports latest NAND Flash interface, and it can support high speed NAND flash requirement as NAND flash increasing capacity.

3.1. Feature

● Host interface:
  ■ PCIe Gen3 x4 (4GB/s bandwidth)
  ■ Compliance with PCIe Gen I(2.5Gbps),Gen II(5Gbps) ,Gen III(8Gbps)
  ■ Compliance with PCI Express Base Specification Revision 3.1
  ■ Compliance with NVMe 1.4
● Flash interface support:
  ■ Support up to Toggle 3.0/ONFI 4.0 interface
  ■ Supply Voltage of FLASH I/O: 1.2V/1.8V
  ■ Transfer rate: Up to 800 MT/s
  ■ Support up to 4 channels/16 Chips Enable (CE)

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- NAND flash support:
    - Support Low Density Parity Check (LDPC) code
    - Support RAID 5 protection
    - Support 3D SLC/MLC/TLC/QLC NAND type flash
    - Support flash with 8KB/16KB page architecture
    - Support four-plane operation
    - Support Toggle Mode flash
    - Support ONFI3.0/ONFI2.3/ONFI2.2/ONFI2.1/ONFI2.0 flash
    - Support ONFI4.1 interface
        - SDR up to mode 5
        - NV-DDR up to mode 5
        - NV-DDR2/3 up to mode 12
- Architecture
    - Built-in 32-bit microcontroller
    - Built-in 1.75MB SRAM
    - Built-in voltage detector
    - Built-in UART function
    - Support JTAG interface
    - Support GPIO
    - Support I2C interface
    - Support AES 128/256
    - Support SHA160/256/512
    - Support RSA2048
    - Support End-to-End data path protection
    - Enhance data with SmartFlush/GuaranteedFlush/SmartRefresh
    - Support smart sudden power cycling handling
    - Support static and dynamic wear leveling algorithm
    - Enhanced ESD design
- Power save implementation
- Operating temperature
    - Commercial grade: 0℃ ~ 70℃
    - Industrial grade: -40℃ ~ +85℃

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- Package
  - Support LFBGA (12 x12x1.3 mm) 288-ball package
  - Lead-free and RoHS compliant

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3.2. AS2263 Function Block Diagram
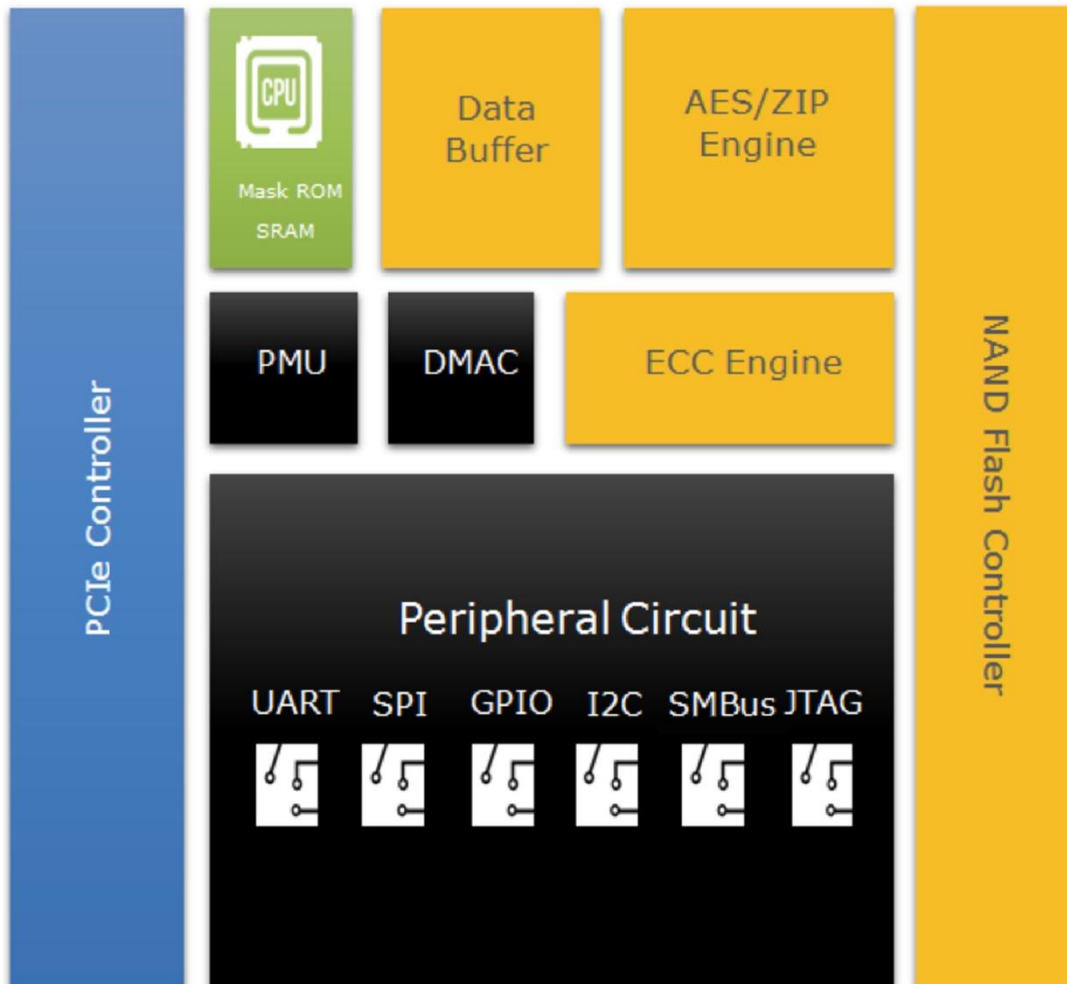
The following diagram is the internal block diagram of AS2263.

Figure 3-1 AS2263 Function Block Diagram

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